## Claims

**What is claimed is:**

1. A circuit comprising:

a master delay line coupled to a first clock having a first clock frequency wherein said master delay line is comprised of a first plurality of delay elements; and

a slave delay line used in conjunction with a second clock domain having a second clock frequency wherein said slave delay line is comprised of a second plurality of delay elements,

wherein said first clock frequency is faster than said second clock frequency and wherein said slave delay line is calibrated to said master delay line.

2. The circuit of claim 1 further comprising:

master calibration logic for measuring a first number of delay elements of said first plurality of delay elements that in sequence provide a predetermined delay amount within said master delay line; and

slave gear logic coupled to said master calibration logic for determining a second number of delay elements of said second plurality of delay elements that in sequence provide said predetermined delay amount within said slave delay line.

3. The circuit of claim 2 wherein said second clock frequency is a multiple of said first clock frequency and wherein said slave gear logic comprises:

a multiplier to multiply said first number of delay elements by said multiple to determine said second number of delay elements.

4. A system comprising:

a first clock having a first clock frequency;

a master delay line coupled to said first clock and comprising a plurality of

delay elements for selectively generating a predetermined master delay amount;

master calibration logic coupled to said master delay line for providing a calibration value indicative or a number of delay elements selected within said master delay line to generate said predetermined master delay amount; and

a plurality of slave components coupled to said master calibration logic wherein each slave component comprises:

a slave delay line comprising a plurality of delay elements for selectively generating a predetermined slave delay amount;

a second clock having a second clock frequency wherein said second clock frequency is less than said first clock frequency;

slave functional circuits coupled to said second clock and coupled to said slave delay line to utilize said predetermined slave delay amount for generating a phase offset between a first signal and a second signal used within said slave functional circuits; and

slave gear logic coupled to said master calibration logic and coupled to said slave delay line for determining from said calibration value a number of delay elements to be selected within said slave delay line to provide said predetermined slave delay amount.

5. The system of claim 4 wherein said slave gear logic comprises:

a multiplier for multiplying said calibration value by a predetermined value to determine said number of delay elements selected within said salve delay line to generate said predetermined slave delay amount.

6. A memory controller including:

a first clock having a first clock frequency;

a master delay line coupled to said first clock and comprising a plurality of delay elements for selectively generating a predetermined master delay amount;

master calibration logic coupled to said master delay line for providing a calibration value indicative or a number of delay elements selected within said master delay line to generate said predetermined master delay amount; and

a plurality of slave components coupled to said master calibration logic wherein each slave component comprises:

a slave delay line comprising a plurality of delay elements for selectively generating a predetermined slave delay amount;

a second clock having a second clock frequency wherein said second clock frequency is approximately half of said first clock frequency;

slave functional circuits coupled to said second clock and coupled to said slave delay line to utilize said predetermined slave delay amount for generating a phase offset between a first signal and a second signal used within said slave functional circuits; and

slave gear logic coupled to said master calibration logic and coupled to said slave delay line for determining from said calibration value a number of delay elements to be selected within said slave delay line to provide said predetermined slave delay amount.

7. The memory controller of claim 6 wherein said slave gear logic comprises:

a multiplier for multiplying said calibration value by two to determine said number of delay elements selected within said salve delay line to generate said predetermined slave delay amount.

8. A method operable with a circuit having a first clock, a second clock, a master delay line coupled to said first clock and a slave component coupled to said second clock wherein said second clock has a lower frequency than said first clock and wherein said slave component includes a slave delay line, said method comprising the steps of:

calibrating said master delay line to determine a calibration value indicating a number of delay elements within said master delay line required to generate a predetermined master delay amount;

determining from said calibration value a corresponding number of delay elements within said slave delay line required to generate a predetermined slave delay amount; and

selecting said number of delay elements within said slave delay line to generate said predetermined slave delay amount from said slave delay line.

9. The method of claim 8 wherein the step of determining includes the step of:

multiplying said calibration value by a multiplier value to determine said number of delay elements within said slave delay line.

10. The method of claim 9 wherein the step of multiplying includes the step of:

multiplying said calibration value by a value substantially equal to the ratio of said first clock frequency to said second clock frequency.